REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claims 1, 9, 21 and 24 are currently being amended. No new matter is added.

This amendment changes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 1-16 and 21-24 remain pending in this application.

In paragraph 1 of the Office Action, the Examiner has objected to the Specification. Applicants have amended the Specification in accordance with the Examiner's comments. Accordingly, withdrawal of the objection of the Specification is respectfully requested.

In paragraphs 2 and 3 of the Office Action, claims 1-16 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,835,246 (Zaidi). The Examiner states:

> Regarding claim 1, Zaidi, (see figures 1-17, col. 7-11, col. 1-67), disclose a method of manufacturing an integrated circuit substrate 22 including a strained layer 28, the method comprising: providing a base layer 32; providing an insulating/dielectric layer 26 above the base layer; providing a semiconductor layer 34, 12, 26, 38, 42, 44, 46 above the insulating layer (see figures 1-5); and forming a plurality of pillars 12a, 12b in the base layer 32a, 32b (see figures 3, 15).
>
> Regarding 2-8, Zaidi, (see figures 1-21, col. 1-67), also teaches providing a compressive material 46 in apertures/grooves associated with the pillars; planarizing the compressive material 46 until the base layer is reached; the semiconductor layer 60a-60a-60d (see figure 15) includes silicon; the insulation/dielectric layer 26 includes silicon oxide/dioxide; the base layer includes silicon;

> wherein the pillars 12 have a width thickness of angstroms; the compressive material 46, 60, 74 includes nitride.
>
> Regarding claim 9, Zaidi, (see figures 1-17, col. 7-11, col. 1-67), disclose a method of forming a strained semiconductor layer 28 above a base layer, the method comprising: etching a plurality of trenches 44a-44b in the base layer 32; and providing a compressive material 46 in the trenches (see figures 3, 5).
>
> Regarding claims 10-16, Zaidi, (see figures 1-21, col. 1-67), also teaches providing a liner 42, 62 in the trenches; providing a mechanical compressive force on the base layer; where the trenches in a waffle pattern, the compressive material is a thermal resistance material and includes nitride; a buried oxide/dioxide layer 26 is between the base layer and the strained semiconductor layer; wherein the semiconductor layer is silicon.

Applicants respectfully traverse the rejection.

In paragraph 4 and 5 of the Office Action, claims 21-24 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,803,631 (Dakshina-Murthy). The Examiner states:

> Regarding claim 21, Dakshina-Murthy, (see figure 4A, col. 10-31), teaches a method of making a substrate 100, the substrate including a strained layer 305 and a base layer 210, 215 below the strained layer, the method comprising: forming trenches 205 on a side opposite the strained layer, the trenches including stress in the strained layer (see col. Lines 1-9). Regarding claims 22-24, Dakshina-Murthy, (see figures 1-6, col. 1-67), also teaches the strained layer is silicon; providing compressive material in the trenches; providing a buried oxide 110 between the strained layer and the base layer.

Applicants respectfully traverse the rejection. Dakshina-Murthy and Zaidi are referred to below as the cited art.

With respect to independent claim 11, independent claim 11 recites:

> pillars extend closer to perpendicular than parallel to the base layer, wherein the pillars have a height greater than a width and wherein the base layer includes a top surface, a top surface being opposite the base layer and for including active components.

Accordingly, the substrate in claim 1 has the top surface for active components which is on an opposite side to the surface for the pillars.

In direct contrast to this structure, Zaidi discloses that the active components are provided on the same side as the pillars. Indeed, Zaidi describes its invention as follows:

> Briefly, the present invention includes a method for improving heteroepitaxial growth of epilayers in lattice expansion-coefficient-mismatched systems by generating micro- and nanoscale walls, columns, films and V-grooves on the surface of a Si or other suitable substrates such that during epitaxial growth, strain energy is predominantly confined in these structures and defects are gettered.

See Zaidi, column 6, lines 55-60.

The epitaxial layers are utilized for forming the active devices on the sides of the trenches. This is in direct opposition to the structure recited in claim 1. Dakshina-Murthy suffers from the same deficiency. FIN 205 is provided for receiving the active devices. Accordingly, FIN 205 cannot be the trench recited in claim 1. Accordingly, claim 1 and its dependent claims 2-8 are patentable over the cited art.

With respect to independent claim 9, claim 9 recites that the strained semiconductor layer has a top surface for active devices, the top surface being opposite the base layer. Such a structure is not shown, described or suggested in the cited art.

As discussed above, both Zaidi and Dakshina-Murthy provide active devices on what the Examiner characterizes as the trench side of the device. This is completely opposite to the principles of the present invention. Accordingly, independent claim 9 and its dependent claims 10-15 are patentable over the cited art.

With respect to independent claim 21, claim 21 recites the step of forming trenches on a side opposite the top surface of the substrate, the top surface being a surface for active devices. As discussed above, both Zaidi and Dakshina-Murthy disclose a structure which is directly opposite to that recited in claim 21. Accordingly, independent claim 21 and its dependent claims 22-24 are patentable over the cited art.

* * * * *

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 06-1447.

Respectfully submitted,

Date 4-21-05

By _____

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